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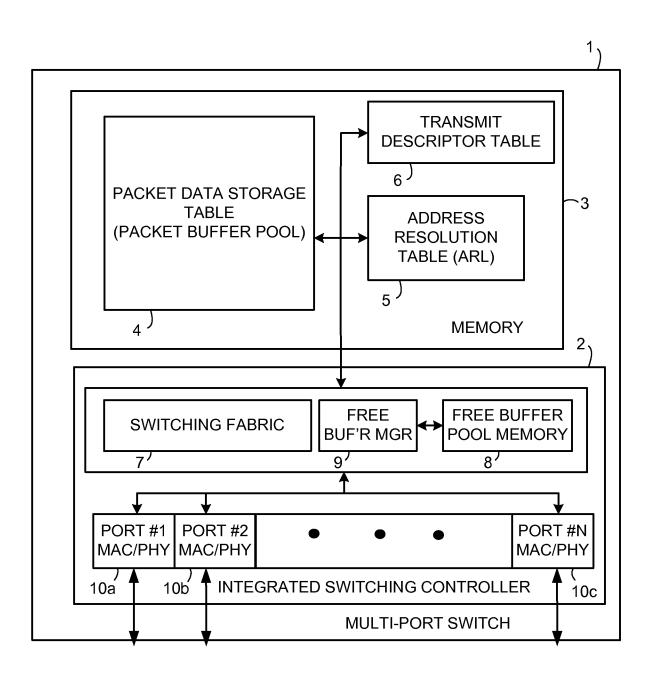


FIG. 1

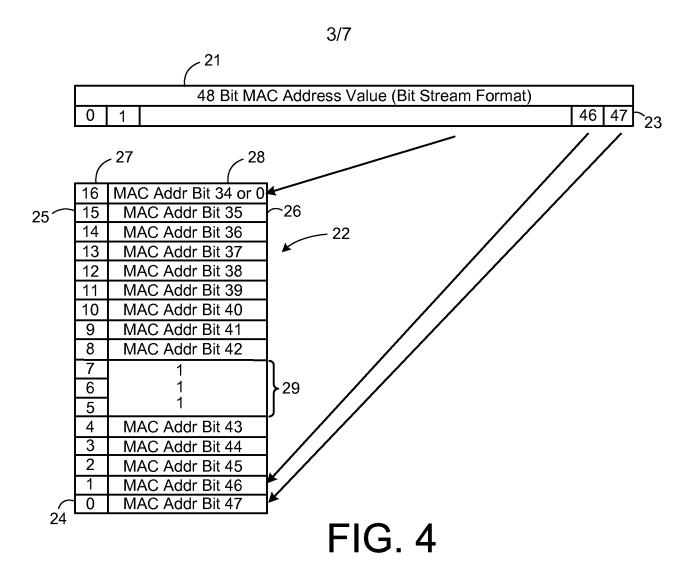
2/7

	Address[7:0]	Data[63:0]	
11-	00-CF	Packet Data	<del></del> 12
13	D0	Port 0 Transmit Descriptor	14
	D1	Port 1 Transmit Descriptor	
	D2	Port 2 Transmit Descriptor	100
	D3	Port 3 Transmit Descriptor	
	D4	Port 4 Transmit Descriptor	
	D5	Port 5 Transmit Descriptor	
	D6	Port 6 Transmit Descriptor	
	D7	Port 7 Transmit Descriptor	
15	D8	Port 8 Transmit Descriptor	<del></del> 16
	D9-DF	Unused	
17	E0-FF	32 ARL Table Entries	<del></del> 18

FIG. 2

	Address[16:0]	Data[63:0]	
19	0000-00FF	Memory Block 0	20
	0100-01FF	Memory Block 1	
	0200-02FF	Memory Block 2	
	0300-FEFF	Memory Block 3 to 2046	
	FF00-FFFF	Memory Block 2047	
	10000-1FFFF	Optional Memory Block 2048-4095	

FIG. 3



	31		<b>√</b> <sup>30</sup>				32 (		
	Address[7:0]	Data[63:0]							
33		[63:56]	[55:48]	[47:40]	[39:32]	[31:24]	[23:16]	[15:8]	[7:0]
	00	В0	B1	B2	В3	B4	B5	В6	B7
	01	B8	B9	B10	B11	B12	B13	B14	B15
		-	-	-	-	-	-	-	-
	07	B56	B57	B58	B59	B60	B61	B62	B63
	80	B64	B65	Unused					
	08-CF			Unused					
		;	{ 34	F	IG.	5	) 36	/ 35	

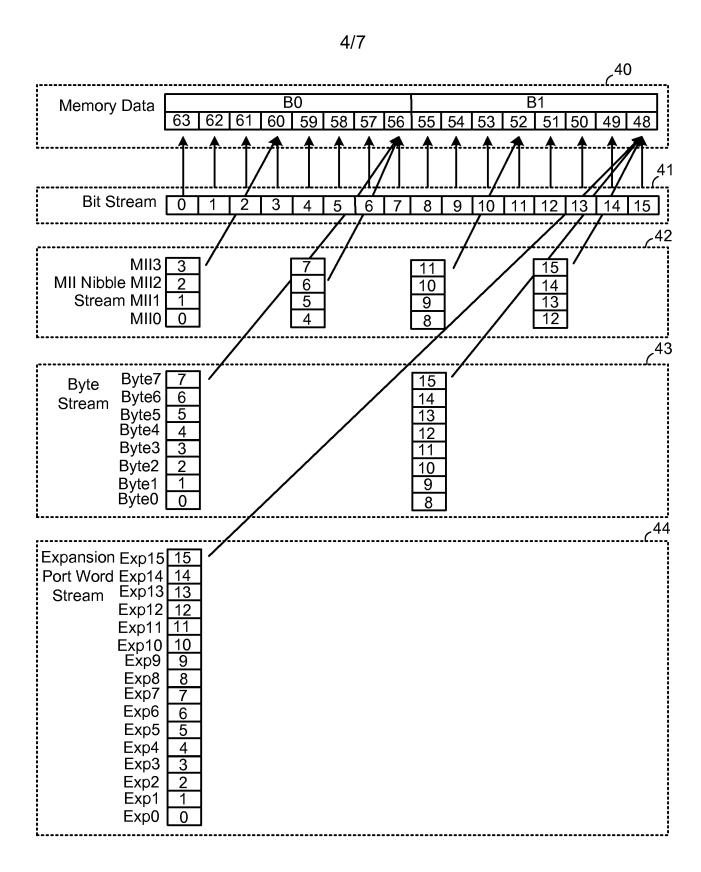
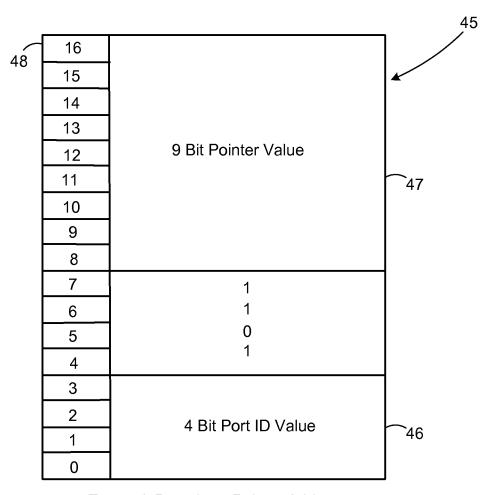


FIG. 6

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Transmit Descriptor Pointer Address

FIG. 7

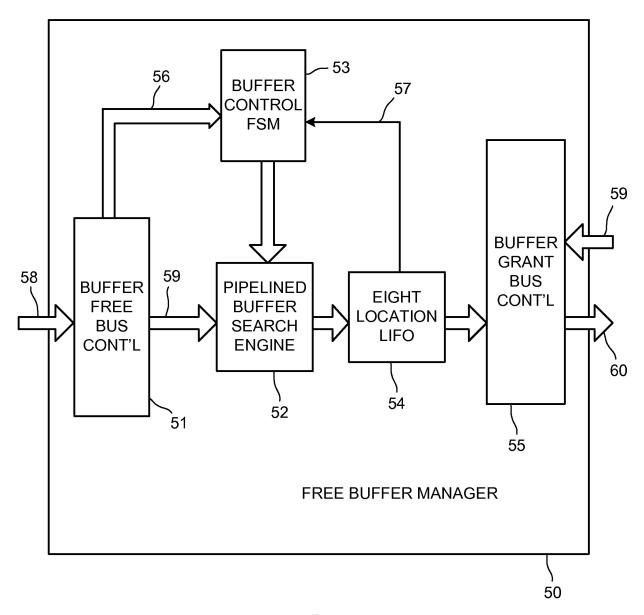


FIG. 8

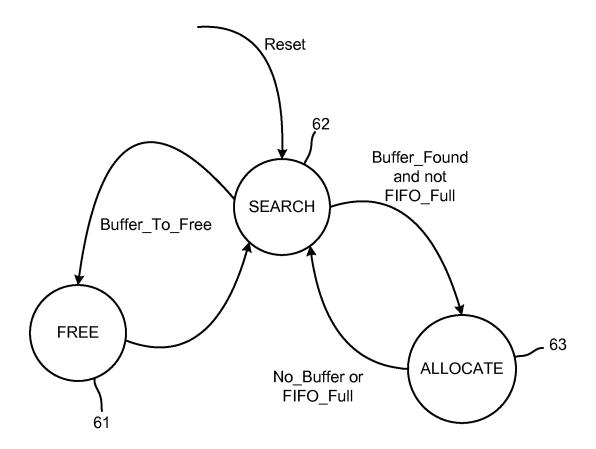


FIG. 9